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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,639	12/30/2003	Brian J. Campbell	BP2231CON	2143

34399 7590 03/30/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,639	CAMPBELL, BRIAN J.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,10-15 and 19-21* is/are rejected.

7)☒ Claim(s) *3 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-7, 13-15, 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Klass (5,917,355).

Klass shows:

1. An apparatus comprising: a converter circuit, including a first pair of complementary metal-oxide- semiconductor (CMOS) transistors (P2, P3, Fig. 7) coupled to be gated by a dynamic logic input signals (X), to generate a static logic output signal on an output node (Q) responsive to the dynamic logic input signal during an evaluate phase of a clock signal, the static logic output signal having a first state or a second state depending on the dynamic logic input signal, the converter circuit further including a first clocked transistor (N4) to enable the first pair of CMOS transistors during the evaluate phases but to float the output node to retain the state of the static logic output signal during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors; and

a noise suppression circuits including a second pair of CMOS transistors (P4, P6) coupled to be gated by a feedback voltage (703) from the output node, to sustain the state of the output node during the precharge phase, the noise suppression circuit

further including a second clocked transistor (P3) which is to be enabled during the precharge phase to couple a first potential (VDD) onto the output node through the second clocked transistor and one (P4) of the second pair of CMOS transistors (through P3 and P4) when the output node is in the first states but to couple a second potential (GND) through the other (N6) of the second pair of CMOS transistors and one (N5) of the first pair of CMOS transistors of the converter circuit when the output node is in the second state (GND through N5 and N6).

2. the apparatus as recited in claim 1 wherein the first clocked transistor is to be active during the evaluate phase of the clock signal and the second clocked transistor is to be active during the precharge phase of the clock signal.

4. The apparatus as recited in claim 2 wherein the first clocked transistor is a NMOS transistor (N4) and the second clocked transistor is a PMOS transistor (P4).

5. The apparatus as recited in claim 2 wherein the first potential placed on the output node is coupled from a supply voltage (VDD) and the second potential placed on the output node is coupled from ground (GND).

6. The apparatus as recited in claim 5 wherein the Converter Circuit operates as an inverter.

7. The apparatus as recited in claim 6 wherein the feedback voltage is an inverted state of the static logic output signal (INV5).

The limitations of claims 13-15, 21 are rejected as above claims.

The apparatus described above is applicable to the method claims 19-20.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-12, 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klass (5,917,355).

Klass discloses the claimed invention except for the transistors of the noise suppression circuit are sized between approximately 30% - 50% of the transistors in the converter circuit or the transistors of the converter circuit and the noise suppression circuit are sized according to an expected noise on the output node. It would have been an obvious matter of design choice to provide the transistors of the noise suppression circuit are sized between approximately 30% - 50% of the transistors in the converter circuit or the transistors of the converter circuit and the noise suppression circuit are sized according to an expected noise on the output node, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art.

Allowable Subject Matter

5. Claims 3 & 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Milshtein et al (6,531,897) discloses a dynamic circuit and static circuit having feedback signal for gating CMOS transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

3/25/05